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Serial No. 10/618,041

Application of: Lee A. Burton

Filed: July 11, 2003

Art Unit:

Examiner:

Attorney Docket No. SRC027

For: SWITCH/NETWORK ADAPTER PORT INCORPORATING SHARED MEMORY RESOURCES SELECTIVELY ACCESSIBLE BY A DIRECT EXECUTION LOGIC ELEMENT AND ONE OR MORE DENSE LOGIC DEVICES
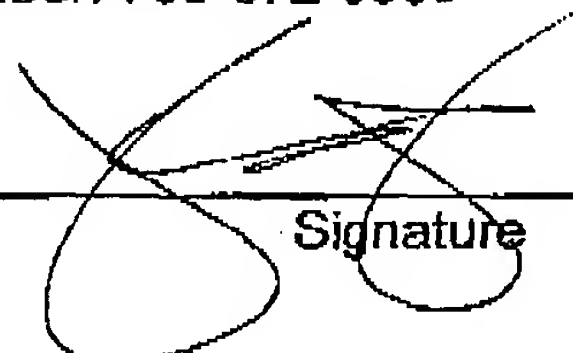
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In re Application of:

Lee A. Burton

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This Information Disclosure Statement is filed before mailing of a first Office Action in the above case. Accordingly, no fee is believed due. However, any fee associated herewith may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

12 December 2003
Date

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U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.[1]	Document No. No. – Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-5,903,771	05/11/1999	Sgro et al.	Figs 1 & 6, col. 3, lines 30-67, col 4, lines 1-51, col 7, lines 1-27.
		US-6,192,439	02/20/2001	Grunewald et al.	Fig 3, col 3, lines 53-67, col 4, lines 1-64.
		US-6,076,152	06/13/2000	Huppenthal et al.	
		US-6,052,773	04/18/2000	DeHon et al.	
		US-5,230,057	07/20/1993	Shido, et al.	
		US-5,892,962	04/06/1999	Cloutier	
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FOREIGN PATENT DOCUMENTS

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		AGARWAL, A., et al., "The Raw Compiler Project", pages 1-12, http://cag-www.lcs.mit.edu/raw, Proceedings of the Second SUIF Compiler Workshop, Augs. 21-23, 1997.	
		ALBAHARNA, OSAMA, et al., "On the viability of FPGA-based integrated coprocessors", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 206-215.	
		AMERSON, RICK, et al., "Teramac—Configurable Custom Computing", © 1995 IEEE, Publ. No. 0-8186-7086-X/95, Pages 32-38.	
		BARTHEL, DOMINIQUE August 25-26, 1997, "PVP a Parallel Video coProcessor", Hot Chips IX, Pages 203-210.	
		BERTIN, PATRICE, et al., "Programmable active memories: a performance assessment", © 1993 Massachusetts Institute of Technology, Pages 88-102.	
		BITTNER, RAY, et al., "Computing kernels implemented with a wormhole RTR CCM", © 1997 IEEE, Publ. No. 0-8186-8159-4/97, Pages 98-105.	
		BUELL, D., et al. "Splash 2: FPGAs In a Custom Computing Machine – Chapter 1 – Custom Computing Machines: An Introduction", Pages 1-11, http://www.computer.org/espress/catalog/bp07413/spls-ch1.html (originally believed published in J. of Supercomputing, Vol. IX, 1995, PP. 219-230.	
		CASSELMAN, STEVEN, "Virtual Computing and The Virtual Computer", © 1993 IEEE, Publ. No. 0-8186-3890-7/93, Pages 43-48.	
		CHAN, PAK, et al., "Architectural tradeoffs in field-programmable-device-based computing systems", © 1993 IEEE, Publ. No. 0-8186-3890-7/93, Pages 152-161.	
		CLARK, DAVID, et al., "Supporting FPGA microprocessors through retargetable software tools", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 195-103.	
		CUCCARO, STEVEN, et al., "The CM-2X: a hybrid CM-2/Xilink prototype", © 1993 IEEE, Publ. No. 0-8186-3890-7/93, Pages 121-130.	
		CULBERTSON, W. BRUCE, et al., "Exploring architectures for volume visualization on the Teramac custom computer", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 80-88.	
		CULBERTSON, W. BRUCE, et al., "Defect tolerance on the Teramac custom computer", © 1997 IEEE, Publ. No. 0-8186-8159-4/97, Pages 116-123.	
		DEHON, ANDRE, "DPGA-Coupled microprocessors: commodity IC for the early 21st century", © 1994 IEEE, Publ. No. 0-8186-5490-2/94, Pages 31-39.	
		DEHON, A., et al., "MATRIX A Reconfigurable Computing Device with Configurable Instruction Distribution", Hot Chips IX, August 25-26, 1997, Stanford, California, MIT Artificial Intelligence Laboratory.	
		DHAUSSY, PHILIPPE, et al., "Global control synthesis for an MIMD/FPGA machine", © 1994 IEEE, Publ. No. 0-8186-5490-2/94, Pages 72-81.	

Substitute for form 1449A/PTO	Application Number	10/618,041
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		ELLIOTT, DUNCAN, et al., "Computational Ram: a memory-SIMD hybrid and its application to DSP", © 1992 IEEE, Publ. No. 0-7803-0246-X/92, Pages 30.6.1-30.6.4.	
		FORTES, JOSE, et al., "Systolic arrays, a survey of seven projects", © 1987 IEEE, Publ. No. 0018-9162/87/0700-0091, Pages 91-103.	
		GOKHALE, M., et al., "Processing in Memory: The Terasys Massively Parallel PIM Array" © April 1995, IEEE, Pages 23-31.	
		GUNTHER, BERNARD, et al., "Assessing Document Relevance with Run-Time Reconfigurable Machines", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 10-17.	
		HAGIWARA, HIROSHI, et al., "A dynamically microprogrammable computer with low-level parallelism", © 1980 IEEE, Publ. No. 0018-9340/80/07000-0577, Pages 577-594.	
		HARTENSTEIN, R. W., et al. "A General Approach in System Design Integrating Reconfigurable Accelerators," http://xputers.informatik.uni-kl.de/papers/paper026-1.html, IEEE 1996 Conference, Austin, TX, Oct. 9-11, 1996.	
		HARTENSTEIN, REINER, et al., "A reconfigurable data-driven ALU for Xputers", © 1994 IEEE, Publ. No. 0-8186-5490-2/94, Pages 139-146.	
		HAUSER, JOHN, et al.: "GARP: a MIPS processor with a reconfigurable co-processor", © 1997 IEEE, Publ. No. 0-08186-8159-4/97, Pages 12-21.	
		HAYES, JOHN, et al., "A microprocessor-based hypercube, supercomputer", © 1986 IEEE, Publ. No. 0272-1732/86/1000-0006, Pages 6-17.	
		HERPEL, H. –J., et al., "A Reconfigurable Computer for Embedded Control Applications", © 1993 IEEE, Publ. No. 0-8186-3890-7/93, Pages 111-120.	
		HOGL, H., et al., "Enable++: A second generation FPGA processor", © 1995 IEEE, Publ. No. 0-8186-7086-X/95, Pages 45-53.	
		KING, WILLIAM, et al., "Using MORRPH in an industrial machine vision system". © 1996 IEEE, Publ. No. 08186-7548-9/96, Pages 18-26.	
		MANOHAR, SWAMINATHAN, et al., "A pragmatic approach to systolic design", © 1988 IEEE, Publ. No. CH2603-9/88/0000/0463, Pages 463-472.	
		MAUDUIT, NICOLAS, et al., "Lneuro 1.0: a piece of hardware LEGO for building neural network systems," © 1992 IEEE, Publ. No. 1045-9227/92, Pages 414-422.	
		MIRSKY, ETHAN A., "Coarse-Grain Reconfigurable Computing", Massachusetts Institute of Technology, June 1996.	
		MIRSKY, ETHAN, et al., "MATRIX: A Reconfigurable Computing Architecture with Configurable Instruction Distribution and Deployable Resources", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 157-166.	

Substitute for form 1449A/PTO			Application Number	10/618,041
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		MORLEY, ROBERT E., Jr., et al., "A Massively Parallel Systolic Array Processor System", © 1988 IEEE, Publ. No. CH2603-9/88/0000/0217, Pages 217-225.	
		PATTERSON, DAVID, et al., "A case for intelligent DRAM: IRAM", Hot Chips VIII, August 19-20, 1996, Pages 75-94.	
		PETERSON, JANES, et al., "Scheduling and partitioning ANSI-C programs onto multi-FPGA CCM architectures", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 178-187.	
		SCHMIT, HERMAN, "Incremental reconfiguration for pipelined applications," © 1997 IEEE, Publ. No. 0-8186-8159-4/97, Pages 47-55.	
		SITKOFF, NATHAN, et al., "Implementing a Genetic Algorithm on a Parallel Custom Computing Machine", Publ. No. 0-8186-7086-X/95, Pages 180-187.	
		STONE, HAROLD, "A logic-in-memory computer", © 1970 IEEE, IEEE Transactions on Computers, Pages 73-78, January 1990.	
		TANGEN, UWE, et al., "A parallel hardware evolvable computer POLYP extended abstract", © 1997 IEEE, Publ. No. 0-8186-8159/4/97, Pages 238-239.	
		THORNBURG, MIKE, et al., "Transformable Computers", © 1994 IEEE, Publ. No. 0-8186-5602-6/94, Pages 674-679.	
		TOMITA, SHINJI, et al., "A computer low-level parallelism QA-2", © 1986 IEEE, Publ. No. 0-0384-7495/86/0000/0280, Pages 280-289.	
		TRIMBERGER, STEVE, et al., "A time-multiplexed FPGA", © 1997 IEEE, Publ. No. 0-8186-8159-4/97, Pages 22-28.	
		UEDA, HIROTADA, et al., "A multiprocessor system utilizing enhanced DSP's for image processing", © 1988 IEEE, Publ. No. CH2603-9/88/0000/0611, Pages 611-620.	
		VILLASENOR, JOHN, et al., "Configurable computing", © 1997 Scientific American, June 1997.	
		WANG, QUIANG, et al., "Automated field-programmable compute accelerator design using partial evaluation", © 1997 IEEE, Publ. No. 0-8186-8159-4/97, Pages 145-154.	
		W.H. Mangione-Smith and B.L. Hutchings. Configurable computing: The Road Ahead. In Proceedings of the Reconfigurable Architectures Workshop (RAW'97), pages 81-96, 1997.	
		WIRTHLIN, MICHAEL, et al., "The Nano processor: a low resource reconfigurable processor", © 1994 IEEE, Publ. No. 0-8186-5490-2/94, Pages 23-30.	
		WIRTHLIN, MICHAEL, et al., "A dynamic instruction set computer", © 1995 IEEE, Publ. No. 0-8186-7086-X/95, Pages 99-107.	
		WITTIG, RALPH, et al., "One Chip: An FPGA processor with reconfigurable logic", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 126-135.	

Substitute for form 1449A/PTO	Application Number	10/618,041
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		YAMAUCHI, TSUKASA, et al., "SOP: A reconfigurable massively parallel system and its control-data flow based compiling method", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 148-156.	
		"Information Brief", PCI Bus Technology, © IBM Personal Computer Company, 1997, Pages 1-3.	
		YUN, HYUN-KYU AND SILVERMAN, H. F.; "A distributed memory MIMD multi-computer with reconfigurable custom computing capabilities", Brown University, 10-13 Dec. 1997, pp. 7-13.	

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